IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	Atty. Docket: NL 021492
JOHANNUS WILHELMUS WEEKAMP ET AL.	Group Art Unit: 2823
Serial No. 10/539,314	Examiner: SINGAL, A.K.
Filed: JUNE 15, 2005	Confirmation No. 2479

Title: ELECTRONIC DEVICE HAVING IMPROVED ISOLATION AND METHOD OF MANUFACTURING SAME (As Amended)

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APPEAL BRIEF

Sir:

Appellants herewith respectfully present a Brief on Appeal as follows, having filed a Notice of Appeal on August 31, 2007:

REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of record Koninklijke Philips Electronics N.V., a corporation of The Netherlands having an office and a place of business at Groenewoudseweg 1, Eindhoven, Netherlands 5621 BA.

RELATED APPEALS AND INTERFERENCES

Appellants and the undersigned attorney are not aware of any other appeals or interferences which will directly affect or be directly affected by or having a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-12 are pending in this application, where Claims 11 and 12 are Withdrawn. Claims 1-10 are rejected in the Final Office Action mailed May 31, 2007. This rejection was upheld, in an Advisory Action that mailed October 2, 2007. Claims 1-10 are the subject of this appeal.

STATUS OF AMENDMENTS

Appellants filed on July 12, 2007 an after final amendment in response to a Final Office Action mailed May 31, 2007. The after final amendment did not include any amendments to the claims. In an Advisory Action mailed on October 2, 2007, it is indicated that the after final amendment filed on July 12, 2007 does not place the application in condition for allowance. This Appeal Brief is in response to the Final Office Action mailed May 31, 2007, that finally rejected claims 1-10, which remain finally rejected in the Advisory Action mailed on October 2, 2007.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention, for example, as recited in independent claims 1 and 8, is directed to an electronic device and a method of manufacturing thereof. As shown in FIG 1D, and described on page 8, line 28, to page 9, line 22, the electronic device 90 includes a substrate 10 having a first layer 1 of an electroconductive material, such as copper, in which first layer 1 conductors 12, 13, 14 (also shown in FIGs 1A-1B) are or will be defined in accordance with a desired pattern.

As also shown in FIG 1D, and described on page 9, lines 23-28, a foil 40 is provided, where the foil 40 has a second patterned layer 2 of electroconductive material. In the second layer 2, conductors are defined in accordance with a desired pattern.

As shown in FIG 1C, and described on page 9, lines 10-22, elements, including a semiconductor element 20 and a first connection element 30, are providing on the first side 101 (FIG 1A) of the substrate 10, thereby bringing into electric contact at least two of these elements 20, 30, one of which is the first connection element 30, and corresponding conductors in the first

layer 101.

As shown in FIG 1D, the foil 40 is provided on either side of the elements 20, 30, thereby establishing electric contact between at least the two elements 20, 30 and the corresponding conductors in the second layer 2.

As shown in FIG 1D-1E, and described on page 9, line 23, to page 10, line 6, a passivating or isolating material 41 is provided from the second side 2 of the semiconductor element through the foil 40. The passivating material 41 forms an encapsulation 50 of the elements 20, 30. Further, the assembly of the substrate 10, the encapsulation 50, and the second conductive layer 2 are separated, thereby forming the electronic device 90.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1 and 8 of U.S. Patent Application Serial No. 10/539,314 are unpatentable under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 6,324,072 (Lorentz) in view of U.S. Patent Application Publication No. 2002/0117743 (Nakatani).

Appellants respectfully request the Board to address the patentability of independent claims 1 and 8, and further claims 2-7 and 9-10 as depending from independent claims 1 and 8, based on the requirements of independent claims 1 and 8. This position is provided for the specific and stated purpose of simplifying the current issues on appeal. However, Appellants herein specifically reserve the right to argue and address the patentability of claims 2-7 and 9-10 at a later date should the separately patentable subject matter of claims 2-7 and 9-10 later become an issue. Accordingly, this limitation of the subject matter presented for appeal herein, specifically limited to discussions of the patentability of independent claims 1 and 8 is not intended as a waiver of Appellants' right to argue the patentability of the further claims and claim elements at that later time.

ARGUMENT

Claims 1 and 8 are said to be unpatentable over Lorentz and Nakatani.

Lorentz is directed to a micro-electronic component of sandwich construction. As correctly noted on page 4 of the Final Office Action, Lorentz does not teach or suggest encapsulating and separating the assembly of the substrate. Nakatani is cited in an attempt to remedy the deficiencies in Lorentz.

Nakatani is directed to a component built-in module. It is alleged, at the bottom of page 4 of the Final Office Action, that FIG 7H of Nakatani shows providing a passivating material (from the second side of the semiconductor element) **through the foil**, which passivating material forms an **encapsulation** of the elements, as recited in independent claims 1 and 8. Applicants strongly disagree.

Nakatani discloses forming various layers over each other. In particular, holes are formed in an uncured sheet of thermosetting resin 704 to form vias 705 which are filled with conductive paste and sandwiched between release carriers 700 including wiring

pattern 701, a semiconductor 702 and chip component 702. The resin sheet 704 is cured to form a component built-in core layer 706. Other resin sheets 707, including vias 708 filled with conductive paste and release carriers 710 with components 709, are provided on both sided of the component built-in core layer 706 as shown in FIG 7H where, after heating and pressing, the release carriers 710 are peeled off. (See paragraphs [0067-0073])

There is simply no teaching or suggestion in Lorentz, Nakatani, and combination thereof, of the present invention as recited in independent claim 1, and similarly recited in independent claim 8 (illustrative emphasis provided):

> providing a passivating material from the second side of the semiconductor element **through the foil**, which passivating material **forms an encapsulation of the elements**.

In Nakatani, at best, the only thing that is provided through something is the conductive paste provided in, or arguendo through, the vias 705, 708 of the resin sheets 704, 707. The Nakatani conductive paste in the vias 705, 708 does not form any encapsulation of the elements. Rather the Nakatani conductive paste fills the vias 705, 708, and provides electric contact or

conductive paths. That is, the Nakatani vias 705, 708 filled with the conductive paste does NOT provide isolation; rather the Nakatani conductive paste provides electric contact.

The Nakatani conductive paste is diametrically opposite the passivating material, as recited in independent claims 1 and 8, where the passivating material forms an encapsulation of the elements thus isolating and protecting the inventive electronic device, where the passivating or isolating material is provided through the foil forms an encapsulation of the elements.

Illustratively, the passivating or isolating material for the encapsulation may "include glass epoxides, acrylates, polyimides but also sol-gel materials that can be cured to glass," as recited on page 3, lines 23-24 of the present application. Thus, the Nakatani **conductive** paste teaches away from the "passivating material [that] forms an encapsulation of the elements," where the "passivating material [is provided] from the second side of the semiconductor element through the foil," as recited in independent claim 1, and similarly recited in independent claim 8.

Accordingly, it is respectfully submitted that independent

claims 1 and 8 are allowable, and allowance thereof is respectfully requested. In addition, it is respectfully submitted that claims 2-7 and 9-10 should also be allowed at least based on their dependence from independent claims 1 and 8.

In addition, Appellants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Appellants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

CONCLUSION

Claims 1-10 are patentable over Lorentz and Nakatani.

Thus, the Examiner's rejections of claims 1-10 should be reversed.

Respectfully submitted,

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CLAIMS APPENDIX

1.(Original) A method of manufacturing an electronic device comprising the steps of:

providing a substrate having a first layer of an electroconductive material, in which layer conductors are or will be defined in accordance with a desired pattern;

providing a foil having a second patterned layer of electroconductive material, in which layer conductors are defined in accordance with a desired pattern;

providing elements, including a semiconductor element and a first connection element, on a first side of the substrate, thereby bringing at least two of the said elements, one of which is the first connection element, and corresponding conductors in the first layer into electric contact;

providing the foil on either side of the elements, thereby establishing electric contact between at least the two elements and the corresponding conductors in the second layer;

providing a passivating material from the second side of the

semiconductor element through the foil, which passivating material forms an encapsulation of the elements; and

separating the assembly of substrate, encapsulation and second conductive layer, thereby forming the electronic device.

2.(Original) A method as claimed in claim 1, characterized in that the foil comprises a detachable layer which is removed after the foil has been provided on the second side of the semiconductor element.

3.(Original) A method as claimed in claim 1, characterized in that the foil comprises a patterned, electrically isolating layer, the foil being provided in such a manner that the second patterned layer faces the elements.

4.(Original) A method as claimed in claim 1, characterized in that the foil comprises an electrically isolating gauze, the foil being provided in such a manner that the second patterned layer faces the elements.

5.(Original) A method as claimed in claim 1, characterized in that a substrate is used in which the connection conductors are already defined in the first layer.

6.(Original) A method as claimed in claim 5, characterized in that the substrate comprises a sacrificial layer which is at least partly removed after the provision of the passivating material.

7.(Original) A method as claimed in claim 1 or 5, characterized in that the passivating material also encapsulates the second patterned layer, and that the substrate has contact faces for external contacting which are situated on a second side facing away from the first side.

8.(Previously Presented) An electronic device with a first side and a second, opposite side that is provided with a semiconductor element having a first and a second connection region that is situated between a first and a second patterned layer of

electrically conductive material on, respectively, the first and the second side, which patterned layers are electrically interconnected via at least a first connection element, conductors being defined in accordance with desired patterns in said layers, and the semiconductor element being electrically connected with conductors in at least one of said layers by the connecting regions, said device being provided, on the first side, with contact faces for external contacting, said contact faces being electroconductively connected with at least a part of the conductors in the first patterned layer, said elements and said second patterned layer being at least substantially encapsulated by an encapsulation of passivating material provided from said second side of said electronic device through said second patterned layer.

9.(Original) An electronic device as claimed in claim 8, characterized in that the second conductive layer is provided, on the side facing away from the elements, with a patterned isolating layer.

10.(Original) An electronic device as claimed in claim 8, characterized in that the second conductive layer is provided, on the side facing away from the elements, with a gauze of isolating material.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None